Design and Characterization of a Dynamic Bias Latch-type CMOS Comparator

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***Abstract*—Analog-to-digital converters (ADCs) are used in many applications ranging from industrial instrumentation to modern communication systems. An essential building block present in ADCs is the CMOS comparator, which is responsible for comparing two or more signals. Dynamic CMOS comparators are the preferred ones in low-power applications due to its power efficiency. There are many dynamic CMOS comparator architectures present in the literature. This work presents the design and simulation results of a Dynamic Bias comparator. This comparator was designed in a 180-nm CMOS process and is powered by a 1.8V power supply. The power consumption of this comparator is 10 fJ per comparison when clocked at 100 MHz. Also, Monte-Carlo (MC) simulation results indicate that this comparator has an input offset of 1.93 mV.**

I. Introduction

Analog-to-digital converters (ADCs) play an essential role in signal processing, providing an interface between the analog and digital domains [1].

There are many ADC architectures such as flash, successive approximation register (SAR), pipeline and sigma-delta. Each architecture is chosen according to the application specified resolution and sampling frequency. Despite different operation principles, those ADCs previously cited have as common build block the CMOS comparator.

Among the several existing comparator architectures, the Strong-Arm comparator is a very effective architecture as it has fast decisions due to its positive feedback and low input offset. However, the large number of cascaded transistors requires a large voltage headroom, which makes its design for current CMOS technologies using low supply voltages unfeasible [2]. In addition, it suffers from large kick-back noise since it lacks a pre-amplifier preceding the latch. In [3] the Double-tail comparator is introduced. It mitigates this problem by separating the pre-amplifier from the latch stage. In this way, independent control of common-mode current is provided for the pre-amplifier and regeneration time in the latch stage. However, a static consumption per comparison is added to the pre-amplifier stage. The strategy found to reduce this consumption is to use the dynamic biasing technique in the pre-amplifier stage, so it is possible to reach a certain signal-to-noise ratio (SNR) with lower consumption [4].

Other CMOS comparator architectures have been introduced in the literature in the recent years such the Elzakker's comparator [5], the Dynamic Bias Latch-Type Comparator [6] and Chevella's comparator [7]. Each comparator presents intrinsic advantages either in speed, delay time or input noise.

This paper aims to show a complete comparator characterization. The Dynamic-Bias Latch-type has been chosen as a case study. Thus, this work presents the characterization of a Dynamic-Bias Latch-type comparator in a traditional 180nm CMOS technology.

The remaining of this paper is organized as follows: Section II presents the comparator architecture; Section III presents the input offset characterization approach; Section IV presents the simulation results; and Section V provides the conclusions and final remarks.

II. Dynamic Bias Latch-Type Comparator

The comparator architecture explored in this work is shown in Fig. 1. It is composed of a pre-amplifier stage (transistors M1-M5) and a latch stage (transistors M6-M13). The main focus of this topology is to reduce the per-bit energy comparison for a given SNR [6]. Thus, the traditional current tail of the pre-amplifier is replaced by a tail capacitor and a tail transistor (M3a), which plays the role of a switch.

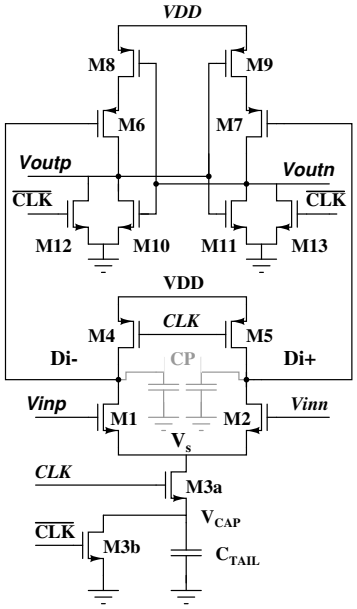


Fig. 1: Dynamic Bias Comparator topology.

Since this comparator is dynamic, it has two operation phases: reset and regeneration. In the reset phase, when the clock is at logic level zero and the pair of transistors M4 and M5 are conducting, the drain nodes ($Di+, Di-$) are pre-loaded to VDD. Transistors M12 and M13 reset the latch and CTAIL is offloaded to GND via M3b. The comparison phase occurs when $CLK = VDD$. Reset transistors (M3b, M4, M5, M12, and M13) are turned off, transistor M3a turns on and the capacitances at $Di+$ and $Di-$ start to discharge.

In this discharge of the CPs (parasitic capacitance present in the DI nodes summed to a small physical capacitor), the common mode current resulting from this process generates a tail current (ITAIL), which loads the CTAIL. As the VCAP voltage increases, the node voltage VS follows, which reduces the VGS of the pair differential M1 and M2, generating a dynamic bias for the differential pair during the comparison phase. The VGS of M1 and M2 decrease until the source voltage achieves its first extinction point, given by VS = min(Vinp - VT, Vinn - VT), where the threshold voltage (VT) is the threshold of M1 and M2. From that point, one of the transistors of the input pair (M1/M2) turns off and the drain voltage in this transistor ceases (considering no subthreshold conduction [4]). The remaining transistor continues to discharge from its CP until the second point, VS = max(Vinp - VT, Vinn - VT). The comparison is made after the second point.

The inverter located on the side that discharged first forces the inverter on the opposite side to inversion. For the dynamic polarization comparator, voltages VD1 and VD2 at nodes Di+ and Di-, at the end of the comparison phase, depend on the value of the load transferred to CTAIL. The energy required by the preamp in the dynamic bias comparator to preload the drain nodes is given as $2 \cdot CP \cdot VDD^2 - CP \cdot VDD \cdot (VD1 + VD2)$. To minimize the effect of noise on the first stage of the preamp [8] [9], the capacitance (CP) must be adequately dimensioned for the desired SNR. Thus the noise power is inversely proportional to the CP. Regarding the power consumption of the comparator, the pre-amplifier is responsible for 70 to 80 percent of the total power consumption [7], whereas reducing this rate by partially discharging the pre-amplifier output is a simple and effective way to reduce power consumption.

A. Design of Dynamic bias latch-type comparator

The circuit sizing can be split in modules. Transistors M5-M10 and M9-M11 compose CMOS inverters fed back to each other. In this way, the sizing of these transistors can follow the basic design of a CMOS inverter [10].

Transistors M6, M7, M12, and M13 are switches and can use the same sizing of inverters, so M11=M10=M12=M13 and M6=M7=M8=M9. The M4 and M5 transistors are switches that need to have a high current capacity to recharge the CP capacitors in half-cycle of clock. The tail transistor M3a has minimum size and has an important function in the circuit, as it can be considered as a key to creating a path between VDD and CTAIL and simultaneously plays the role of the current source to bias the pre-amp at the beginning of comparator operation. Transistor M3b is responsible for discharging the CTAIL capacitor, having the ability to fully discharge the tail capacitor in half-cycle of clock.

For the tail capacitor (CTail), the simulation and the dimensioning of the equivalent capacitance of the node (CP) were carried out, and thus a relation between the parasitic capacitances and the tail capacitor of CP/CTAIL = 0.35 was obtained. It is worth mentioning that this interaction between the capacitances has a fundamental role in this applied technique, because when unloading CP to CTAIL it would create an ITAIL current. For the transistors, the sizing was performed through 500 Monte Carlo runs, seeking a standard deviation of the offset voltage of less than 5 mV. Tab. I presents the obtained transistors/capacitors sizes.

TABLE I: Obtained sizes for transistors and capacitors of the Dynamic Bias comparator of Fig. 1.

Transistors	**W/L(μm)**	**Multiplier**
Input pair (M1/M2)	40.0/0.18	1
From M4 to M9	2.75/0.18	5
From M10 a M13	1.0/0.18	1
M3a	2.0/0.18	1
M3b	25.0/0.18	1
Capacitor	**(fF)**	
CTail	25	

B. Auxiliary NOR-type SR latch

A simple NOR-based SR-latch logic circuit is connected to the comparator outputs, as shown in Fig. 2. This circuit is used to supress the regeneration transient of the comparator output response. As long as the Voutn and Voutp inputs are low, the feedback keeps A and B in constant state, with the B complement of A. If Voutn (Set) is logic high while Voutp (Reset) is low, then output A is forced logic high , remaining high when Voutn returns to low. If Voutp is high while Voutn is low, output A will be low and will remain low when Voutp returns low [11].

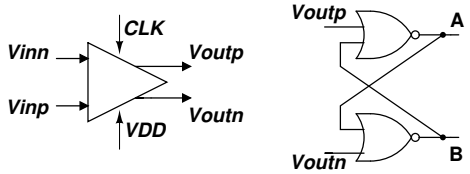


Fig. 2: Comparator and latch SR.

III. Input offset characterization

The comparator is a circuit that compares analog or reference signals and generates a binary signal based on the performed comparison. One of the main comparator non-idealities is the input-referred offset, referred as comparator offset along this paper. The comparator offset is highly dependent on process variation, layout asymmetries and transistors sizing. The comparator offset affects directly the differential non-linearity (DNL) and integral non-linearity (INL) as well as the maximum achieved resolution in many Nyquist-rate ADCs.

Ideally, the comparator transition should occur with zero Volts of difference. In practice, an offset appears at the input. The offset voltage is the difference between the point where ideally the comparator transition should occur and where it really does.

The traditional method for checking the offset voltage is through the ramp method, where one of the comparator inputs is applied to a slow ramp while the other receives the common-mode voltage (V_{CM}) [12]. Simulations of comparator circuits are very complicated and time consuming since some comparators employ some hysteresis or some clocking scheme to reduce offset or energy.

The ramp method becomes almost unfeasible when we take into account that long Monte-Carlo simulations are needed for the execution of this technique. In addition, the speed of the comparison and the accuracy of the offset are directly related to the speed of the ramp, depending on its settings.

To speed-up the comparator offset (and histeresis) simulation, Omran has introduced in [13] a fast and accurate technique for comparator offset voltage simulation, called smart resetable SAR (SRSAR). This technique allows the complete offset characterization (Monte Carlo simulation) in few minutes, while the traditional ramp-based methods take a few hours.

The SRSAR technique is implemented in a VerilogA block called Vos Tester, shown in Fig. 3. This block sends all the stimuli necessary for the comparator simulation, thus eliminating any parallel circuit for the testbench, providing the clock signal, input voltage, and supply voltage to the comparator. It evaluates the comparator output throughout the simulation, generating two signals, Vos.R and Vos.F, according to the calculated compensation voltages.

This block can be implemented in any comparator topology. Parameters can be modified as needed. As the clock's active edge time, it can be disconnected for comparators that do not use the clock. Both output and input signals have the option of single or differential termination. If the input is single-ended, Vinn is fixed at a voltage selected by the user, and the stimulus waveform is applied to Vinp, While in the differential input - as the name implies -, the waveform is divided differentially between the two inputs, the two inputs are superimposed at a common-mode voltage chosen by the user. Search resolution and voltage search range can also be chosen.

IV. Simulation Results

This section presents the simulation results of the designed comparator considering a 1.8-V power supply and an input-common-mode voltage (VCM) of 0.9 V. The comparator clock is set to 100 MHz for study of case and the main comparator characteristics are evaluated as described in next subsections.

A. Offset

The extraction of voltage values from the offset for both directions, rising ($V_{os.R}$) and falling ($V_{os.F}$), were obtained through 500 MonteCarlo simulation runs, using the VerilogA (SRSAR) block as a testbench. At the end of these rounds,

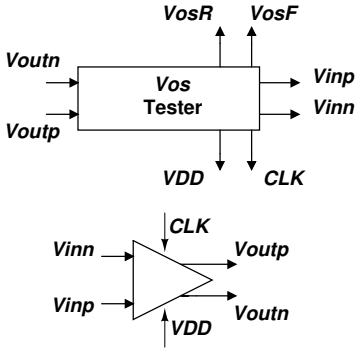
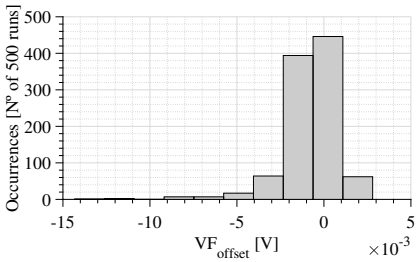
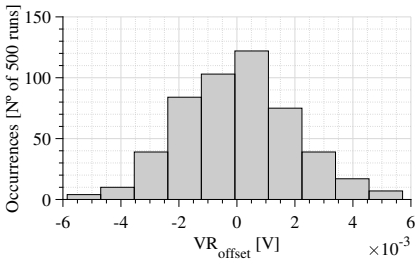


Fig. 3: Vos Tester for comparator testbench.

the histograms, $V_{os.R}$ and $V_{os.F}$, and their standard deviation values are observed, with $V_{os.R}$= 1.939 mV and $V_{os.F}$= 1.938 mV. Considering that the standard deviation is less than 5 mV, the extracted results are satisfactory. The results are shown in Figure 4.



(a) $V_{os.F}$.



(b) $V_{os.R}$.

Fig. 4: Histograms of DoubleTail $V_{os.F}$ and $V_{os.R}$using SRSAR for 500 MC runs.

B. Comparison delay time

For the evaluation of the delay time with respect to the clock, a differential voltage was applied to the VINN input, while the VINP input remained fixed at VCM (900mV). Then, a parametric simulation was performed varying the value of the differential voltage from 1 mV to 1 V. We consider the clock signal as a reference and the output A of the latch SR as the signal to be compared. Starting from the results shown in Figure 5, it can be observed that the delay tends to be smaller and stable when approaching 1 V of differential voltage.

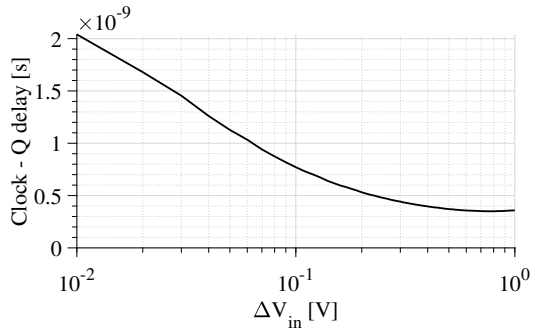


Fig. 5: CLK-Q delay versus the differential input voltage.

C. Energy per comparison

The power consumption by comparison is obtained from the power supply voltage and the integral of the current during a comparison period. The energy per comparison is less than 10 fJ for differential input voltages lower than 1 mV, as shown in Fig. 6.

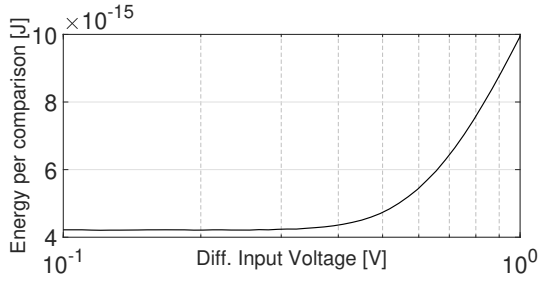


Fig. 6: Energy consumption per comparison of Dynamic Bias latch-type comparator in function of differential input voltage.

D. Input-referred noise

The comparator input-referred noise (IRN) is simulated with a transient-noise simulation considering the maximum noise frequency of 10 times the comparator clock frequency. Figure 7 shows the simulated cumulative probability density distribution (CDF) and its CDF fitting. The fitting was done in Matlab. The comparator IRN is equal to 0.12466 mV, being suitable to keep the INL of a general 12-bit SAR ADCs with a 1.8-V voltage reference within the $\pm 0.5\ LSB$ range.

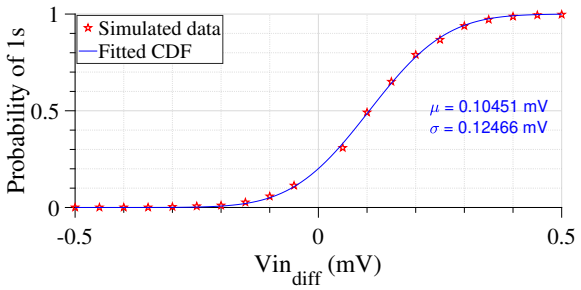


Fig. 7: Simulated cumulative probability density distribution and its CDF fitting.

V. Conclusion

This paper presented the complete sizing and characterization of a Dynamic Bias latch comparator, including power consumption, offset voltage, delay time, and input-referred noise. The energy consumption is equal to 10 fJ per comparison. This low consumption is due to the dynamic biasing technique applied to this topology, a simple and functional solution with low overhead to reduce the power consumption of the pre-amp. An offset voltage with a standard deviation equal to 1.939 mV and 1.938 mV for rising and falling input signals, respectively, were obtained through the analysis performed by the VerilogA block. The CLK-Q delay proved to be reasonable, due to the use of relatively small transistors and strong inversion. The comparator input referenced noise is equal to 0.12609 mV, so for general 12-bit SAR ADCs application it is suitable to conserve the INL.

ACKNOWLEDGMENT

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